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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,864	07/02/2003	Alok Tripathi	42P16617	4391

8791 7590 02/21/2007

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EXAMINER	
ZISKIND, ANNA Y	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,864	TRIPATHI ET AL.	
	Examiner	Art Unit	
	Anna Ziskind	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/12/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 1/12/06 was considered and made of record by the examiner.

Claim Objections

Claims 4-10, 14, 20, and 24 are objected to because of the following informalities: claims 4, 14, 20, and 24 state that "each of the at least two equalization circuits include an RC filter," whereas it should say –each of the at least two equalization circuits includes an RC filter–. Appropriate correction is required.

Claims 28-30 are objected to because of the following informalities:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 10, 17-20, and 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5191300 (Graham et al.).

As to claims 1 and 27, Graham teaches an apparatus that includes an amplifier (Fig. 2, reference 16), a gain circuit (Fig. 2, stages 2-4) that provides four gain values in response to the output of the amplifier, and a control circuit (Fig. 2, reference 25) that provides one of the four gain values (Col. 3, lines 4-26).

As to claims 2, 3, 18, and 19, Graham teaches that the gain circuit includes three equalization circuits, each coupled in series to the output of the amplifier and providing a respective one of the gain values (Fig. 2, stages 2-4).

As to claims 4, 20, and 30, Graham teaches that each of the equalization circuits includes an RC filter (Fig. 3, R and C connected to transistor 61; Col. 5, lines 1-6).

As to claim 10, Graham teaches that the resistance and capacitance values of the RC filter are fixed during circuit design, as evidenced by the specification of these values in Fig. 3.

As to claim 17, Graham teaches a transmitter, receiver, and interconnect (Col. 1, lines 35-36). Graham also teaches that the receiver includes the claimed amplifier, gain circuit, and control circuit, as discussed in the rejection of claim 1.

As to claims 28 and 29, Graham teaches that that each cascaded stage in the gain circuit includes equalizing amplifiers (Col. 3, lines 4-26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5191300 (Graham et al.) in view of US Patent 3906406 (Iwakami).

As to claim 5, Graham doesn't teach that the resistance and capacitance of the RC filter are implemented using on-chip components. Iwakami teaches an equalization system that includes an RC network that is

implemented on an integrated circuit (Col. 2, lines 10-18; Col. 5, lines 37-45). Therefore, it would have been obvious to one of ordinary skill in the art to implement the resistance and capacitance of the RC filter using on-chip components. Doing so would minimize parasitic capacitance and inductance of the circuit (Iwakami, Col. 5, lines 45-48).

As to claim 8, Graham doesn't teach that all the resistors in the apparatus are formed of a same technology. Iwakami teaches an equalization apparatus that is wholly implemented on an integrated circuit (Col. 5, lines 37-45). Because the components of the apparatus of Iwakami are similar to the ones in Graham and the same benefits of integrated circuit implementation discussed in Iwakami would apply in Graham, it would have been obvious to one of ordinary skill in the art to implement the apparatus taught by Graham, including the resistors, through integrated circuit technology. Doing so would decrease parasitic capacitance and inductance in the system (Iwakami, Col. 5, lines 45-48).

Claims 11-14 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5191300 (Graham et al.) in view of US Patent 4837527 (Sauer).

As to claims 11 and 21, Graham teaches that the stages in the amplifier and gain circuit include an MOS transistor (Col. 5, lines 1-6). However, Graham doesn't explicitly teach that the entire amplifier and gain circuit are

implemented in CMOS. Sauer teaches that CMOS is a particularly advantageous type of MOS technology to be used in circuit implementation (Col. 1, lines 24-30). Therefore, it would have been obvious to one of ordinary skill in the art to build a CMOS amplifier and gain circuit, since the transistors in these circuits are already MOS. Doing so would enable relatively high speed operation with lower power consumption (Sauer, Col. 1, lines 28-30).

As to claims 12, 13, 22, and 23, Graham teaches that the gain circuit includes three equalization circuits, each coupled in series to the output of the amplifier and providing a respective one of the gain values (Fig. 2, stages 2-4).

As to claims 14 and 24, Graham teaches that each of the equalization circuits includes an RC filter (Fig. 3, R and C connected to transistor 61; Col. 5, lines 1-6).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5191300 (Graham et al.) in view of US Patent 5955911 (Drost et al.). Graham doesn't teach that the resistance of the RC filter is implemented using passive components. Drost teaches an implementation of resistance using poly-silicon, which is a passive component (Col. 9, lines 1-6). Therefore, it would have been obvious to one of ordinary skill in the art to use poly-silicon to implement a resistance. Poly-silicon is a cheap and easy to integrate method of implementing resistance.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5191300 (Graham et al.) in view of US Patent 4839542 (Robinson). Graham doesn't teach that the resistance of the RC filter is implemented using active components. Robinson discusses the use of active resistance components in a filter implementation (Col. 1, lines 65-68; Col. 2, line 1). Therefore, it would have been obvious to one of ordinary skill in the art to use active components to realize the resistance of an RC filter. Doing so adds the advantage of easy tenability to the filter (Robinson, Col. 1, lines 57-65).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5191300 (Graham et al.) in view of US Patents 3906406 (Iwakami) and 5955911 (Drost et al.). Graham and Iwakami teach that the resistors of the apparatus of Graham are implemented through an integrated circuit, as discussed in the rejection of claim 8. However, neither Graham nor Iwakami teaches that the resistors are implemented using poly resistance technology. Drost teaches that on-chip resistors may be implemented through poly resistance technology (Col. 9, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art to used poly resistance technology to implement the on-chip resistance taught jointly by Graham and Iwakami. Poly-silicon is a cheap and easy to integrate method of implementing on-chip resistance.

Claims 15, 16, 25, 26, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 5191300 (Graham et al.) in view of US Patent

3671886 (Fudemoto et al.). Graham doesn't teach that the control circuit includes a DC feedback circuit. Fudemoto teaches an apparatus for automatic gain control that includes a control circuit with DC feedback, which controls the output of the control circuit (Fig. 2A, reference 20a; Col. 2, lines 37-40). Therefore, it would have been obvious to one of ordinary skill in the art to include a DC feedback circuit with the control circuit of Graham. Doing so would add stability to the circuit by ensuring that its output is always at the correct level.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anna Ziskind whose telephone number is (571) 272-2769. The examiner can normally be reached on Mon. - Fri., 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Anna Ziskind
Examiner
Art Unit 2611

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER